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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/500,623	07/02/2004	Andrew MG Westcott	540-508	2994

23117 7590 02/09/2006

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EXAMINER	
AMAYA, CARLOS DAVID	
ART UNIT	PAPER NUMBER
2836	

DATE MAILED: 02/09/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/500,623	WESTCOTT, ANDREW MG	
	Examiner	Art Unit	
	Carlos Amaya	2836	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07/02/2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26 and 28-34* is/are rejected.

7)☒ Claim(s) *27* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *02 July 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *07/02/2004*
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. Figure 1 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-7,13-14,17-25,28 rejected under 35 U.S.C. 102(b) as being anticipated by Wilcox (US 5,847,554).

With respect to claim 1 Wilcox discloses a switching circuit comprising an input operable to receive a DC signal of +VS (Vin), an output (Vout), first and second switches (Switch MOSFET 342 and 344) operable in response to first and second switching signals to be switched between on and off states (Signals produce by drivers 108 and 112, turns switches on and off) such that switching between various

combinations of on and off states produces an electrical signal at the output with voltage pulses at levels of +VS, 0V and -VS (The turning on and off of the transistor produces a desired output, Column 5 lines 43-57, Column 6 lines 1-6) and a voltage sensor (Sensing circuitry 320) for producing a signal indicative of a voltage offset in the switching circuit (Column 4 lines 57-67) .

With respect to claim 2 Wilcox discloses a switching circuit according to claim 1, wherein the voltage sensor is arranged to measure fluctuations in the DC signal (Sensing circuitry 320 senses changes in the voltage of the switches).

With respect to claim 3 Wilcox discloses a switching circuit according to claim 1, wherein the voltage sensor is arranged to produce a signal indicative of a predicted value of the DC signal (Figure 9, threshold voltage 950 provides a pre-determined value for the operation of the switches. Column 7 lines 49-55).

With respect to claim 4 Wilcox discloses a switching circuit according to claim 3, wherein the voltage sensor includes a finite impulse response filter arranged to measure the DC signal (Figure 9 Filter Capacitor 952 is providing the filtering for the signal supply by the switches 902 and 904).

With respect to claim 5 Wilcox discloses a switching circuit according to claim 1, wherein the voltage sensor is operable to produce a signal indicative of a voltage drop across a diode and/or transistor in the switching circuit (Sensing circuitry 320 senses the voltage drop in the transistors and adjust the switching accordingly. Column 4 lines 57-60).

With respect to claim 6 Wilcox discloses a switching circuit according to claim 5, wherein the voltage sensor is arranged to measure the current flowing through the output (Figure 3 IL current through the inductor is measure by the sensing circuitry 320. Column 5 lines 33-37).

With respect to claim 7 Wilcox discloses a switching circuit according to claim 6, wherein the voltage sensor is operable to produce a signal indicative of a voltage drop across a diode and/or transistor of the switching circuit (Figure 3, Sensing circuitry 320 produces a signal in response to a voltages drop Vds of the transistors) with reference to a measurement of the current flowing through the output (Sensing circuitry 320 also measures IL output current through the inductor) and a value of the resistance of the diode and/or transistor (Rds is the value of the drain to source resistance of the switches).

With respect to claim 13 Wilcox discloses the switching circuit as claimed in claim 1. One skilled in the art would necessary perform the recited method steps of claim 13 when using the equipment disclose above, to perform the functions of the switching circuit to control the voltage to produce a desired value depending upon a change in the output voltage value.

With respect to claim 14 Wilcox discloses the method of claim 13, wherein at least one of the first and second switching signals is generated with reference to a voltage signal indicative of the DC signal such that the at least one first or second switching signal compensates for fluctuations in the DC supply (Figure 9, Column 7 lines 22-23).

With respect to claim 17 Wilcox discloses the equipment as recited in claim 5. One skilled in the art would necessarily perform the recited method steps when using the equipment as describe in claim 5.

With respect to claim 18, Wilcox discloses the equipment according to claim 7. One skilled in the art would necessarily perform the recited method steps when using the equipment as describe in claim 7.

With respect to claim 19 Wilcox discloses the method of claim 13. One skilled in the art would necessarily perform the method step of claim 13, further including a signal generated in response to a slow response times in the first or second switch.

With respect to claim 20 Wilcox discloses the equipment as recited in claim 8. One skilled in the art would necessary perform the recited method steps of claim 20 when using the equipment as described in claim 8.

With respect to claim 21 Wilcox discloses the equipment as recited in claim 9. One skilled in the art would necessarily perform the recited method steps when using the equipment as describe in claim 9.

With respect to claim 22 Wilcox discloses the method of claim 20, wherein the first and second switches are transistors (902 and 904, Figure 9) and the method comprises the step of switching the transistors between on and off states corresponding to substantially maximum (Column 7 lines 16-17) and substantially minimum current flow respectively through the transistor. (Regulator 900 by way of the PWM 912 controls the operation of the transistor between a maximum value and a minimum

value. Figure 10, Column 7 lines 22-25). Figure 9 shows the circuit of figure 3 with the only difference being the sensing circuitry 920 and the inverter 910.

With respect to claim 23 Wilcox discloses the method according to claim 13 comprising the step of generating pulsed first and second signals (Oscillator 104 Figure 3, is a pulsed generator that generate the signals to control the operation of the switches, Column 1 lines 54-65. In figure 9 there is also a PWM 912 that generates a first and second pulsed switching signals that control switches 902 and 904).

With respect to claim 24 Wilcox discloses the method according to claim 23 comprising the step of generating the first and second switching signals according to a rule that the first and second switches are not switched concurrently (Drivers 108 and 112 control the operation of transistors 342 and 344 respectively, depending upon a sense Vds voltage of either transistors. From this operation we know that the transistors are not operated at the same time Column 5 lines 23-25. Regarding Figure 9 there is an inverter 910 ensuring that the transistors 902 and 904 are not switched concurrently Column 7 lines 20-21).

With respect to claim 25 Wilcox discloses the method of claim 23 comprising the step of generating the first and second switching signals according to a rule that the signals are to have no more than one pulse per period (Column 7 lines 22-32).

With respect to claim 28 Wilcox discloses the method of claim 23 comprising the step of generating the first and second switching signals according to a pulse width modulation scheme (PWM 912 In Figure 9).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 8-11,30-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilcox (US 5,847,554) in view of Dyer (US 4,585,986).

With respect to claims 8 Wilcox in view of Dyer discloses a switching circuit according to claim 1 as set forth in the 102 rejection above. Wilcox, however, does not discloses that the switching circuit comprises a bridge circuit, and first and second arms having first and second switches respectively, the first and second arms being connected to opposed ends of the output.

Dyer discloses a bridge arrangement having an input that receives a DC signal of voltage +VS (Battery bank 7 Figure 1), an output (Inductive load 5) and first and second arms having first and second switches (Switch 21 and switch 19), this switches are connected to opposed ends of the output (Figure 1).

At the time of the invention, it would have been obvious to a person of ordinary skilled in the art, to arrange the switching circuit of Wilcox invention to a bridge circuit as disclosed by Dyer.

The suggestion or motivation for doing so would have been to have a more precise control of the output generated by the switches, thus improving the overall voltage supply to the load.

With respect to claims 9-11 Wilcox in view of Dyer discloses the switching circuit according to claim 8. Dyer discloses that the bridge circuit is a half-bridge with third and fourth arms having diodes (Column 3 lines 40-41, line 45). The first and second switches are transistors (Transistor switching device 19 and 21). Comprising an electromagnet connected across the output of the bridge circuit (Figure 1 Inductor 5).

With respect to claim 30 Wilcox in view of Dyer discloses the method of claim 13. Dyer discloses the step of receiving a current demand signal (current measurement device 27) indicative of a desired current to be supplied to the output in a period and calculating the voltage demand signal indicative of a desired voltage of an electrical signal to be supplied to the output during a period (Column 4 lines 3-6, output being control by controller 29 and timing circuits) that results in the electrical signal being supplied to the output during the period with a current substantially equal to the desired current (controller 29 controls the operation of transistors 19 and 21 to produce at the load an output current substantially equal to a desired current).

With respect to claim 31-32 Wilcox in view of Dyer discloses the method of claim 30, the step of calculating the voltage demand signal is performed with reference to a model of the load characteristic of a load connected to the output. Further comprising the step of generating the voltage demand signal with reference to a current signal indicative of a current flowing through the output (Column 4 lines 22-30).

6. Claims 12,15-16,29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilcox (US 5,847,554) in view of Smedley (US 5,559,467).

With respect to claim 12, Wilcox discloses the switching circuit according to claim 1 as set forth in the 102 rejection above. Wilcox does not disclose that the switching circuit comprises a noise shaper operable to noise-shape the first and second signals. Smedley, however, discloses a noise shaper 60 operable to noise-shape the first and second signals produced by the PWM 64 (Figure 4 lines 34-37).

At the time the invention was made, it would have been obvious to a person of ordinary skill in the art, to insert a noise shaper as described by Smedley in the switching circuit of Wilcox.

The suggestion or motivation for doing so would have been to produce a signal free of noise, to obtain a more reliable operation of the switches that is factored into a better supply of power to the load.

With respect to claim 15 Wilcox in view of Smedley discloses the method of claim 14. However, Wilcox does not disclose that the voltage signal is passed through a filter to obtain a predictive measure of fluctuations in the DC supply. Smedley, however discloses a DC signal generated by Switches 40 and 42 pass through a filter arrangement 44 (Figure 9) and then to a noise and ripple shaping chip, which via a PWM controls the operation of the switches (Column 8 lines 25-30).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art, to insert a filter in Wilcox's invention to have a measure of the input voltage.

The suggestion or motivation for doing so would have been to obtain a predictive value of the DC signal in order to adjust the switching circuit to obtain at the output a value that corresponds to the fluctuations of the DC signal, the filtering adds a more precise output voltage.

With respect to claim 16 Wilcox in view of Smedley discloses the method of claim 15, however does not discloses that the voltage signal is passed through a finite impulse response filter. By the teachings of Smedley regarding the low-pass output filter 44, it would have being obvious to one skilled in the art to provide a different filter than the one described by Smedley, in order to obtain a predictive measure of the fluctuations in the DC supply.

With respect to claim 29 Wilcox in view of Smedley discloses the equipment as recited in claim 12. One skilled in the art would necessary perform the recited method steps when using the equipment as described in claim 12.

7. Claims 26, 33-34 are rejected under 35 U.S.C. 103(a) as being unpatentable over Wilcox (US 5,847,554) in view of Ramarathnam (US 6,316,895)

With respect to claim 26 Wilcox discloses the method of claim 23, however, does not disclose that the step of generating the first and second switching signals according to a rule that any pulse should be positioned symmetrically about the centre of the period. Ramarathnam, however, discloses in figure 8 that the pattern of the switching signals is symmetric with respect to the center of the switching period (Column 7 lines 62-67).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art, to perform the step of generating the signals in a symmetric manner with respect to the period.

The suggestion or motivation for doing so would have been to obtain an output signal free of distortions and provide a required output to a load as precise as possible. Ramarathnam teaches that the symmetric PWM is used to produce least harmonics at the output.

With respect to claims 33 and 34 Wilcox discloses the method of claim 13, however, does not disclose a computer program comprising program code means for performing the method steps of claim 13 when the program is run on a computer and/or other processing means associated with the switching circuit. Ramarathnam discloses a software program to control the operation of the switches (Column 3 lines 20-27 and lines 66-67). Wilcox does not disclose a computer program product stored on a computer readable medium. Ramarathnam discloses a micro-controller (5) with a ROM and RAM, and the software program being installed in the ROM (Column 6 lines 29-36).

At the time of the invention, it would have been obvious to a person of ordinary skill in the art, to have a computer program and a computer program product with storing means performed the steps of the invention disclosed by Wilcox.

The suggestion or motivation for doing so would have been to obtain a more precise output voltage with the sensing circuitry of Wilcox, since a computer and computer codes are controlling the voltage generated by the switching circuitry.

Allowable Subject Matter

8. Claim 27 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Claim 27 is allowable over the prior art of record, because the prior art of record does not disclose or suggest "the step of generating the first and second switching signals according to a rule that where pulses cannot be centered symmetrically, the longer and shorter sides of the asymmetric pulses are alternated between the leading edge side and the trailing edge side for successive pulses."

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to the examiner's supervisor, Brian Sircus who can be reached on (571)272-2058. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

PHUONG T. VU
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